CLAIMS

What is claimed is:

1. A computer system, comprising:

a processor capable of executing multiple threads;

an I/O controller coupled to said processor;

an I/O device coupled to said I/O controller; and

a main system memory coupled to said processor;

wherein said processor processes a program in a main thread that includes instructions which cause the processor to spawn a pre-execution thread in which at least a portion of the same program executes, said pre-execution thread runs concurrently with the main thread, but ahead of the main thread in program order.

2. The computer system of claim 1 wherein said instructions that cause the pre-execution thread to be spawned include a start instruction which causes a pre-execution thread to start and a stop instruction which causes the pre-execution thread to stop.

3. The computer system of claim 2 wherein said start instruction includes a value designating the location in the program where the pre-execution thread is to start running.

4. The computer system of claim 1 wherein the pre-execution thread encounters a cache miss condition for a memory reference but the main thread does not encounter a cache miss condition when that same memory reference is processed by the main thread.

5. The computer system of claim 1 wherein said processor determines whether sufficient hardware resources are available before spawning said pre-execution thread.

6. The computer system of claim 1 wherein said processor ignores exception conditions generated during the pre-execution thread.

7. The computer system of claim 1 wherein said processor does not permit a store instruction in the pre-execution thread to modify main system memory contents.

8. The computer system of claim 1 wherein said processor does not permit any store instruction in the pre-execution thread to modify main system memory contents.

9. The computer system of claim 1 further including a buffer into which pre-execution thread stores data is written to make such store data available to pre-execution thread load instructions.

10. A processor, comprising:

a fetch unit capable of fetching instructions from a plurality of threads;

a program counter coupled to said fetch unit;

an instruction cache coupled to said fetch unit;

a data cache coupled to said instruction cache;

wherein said processor processes a program in a first thread that includes instructions which cause the processor to spawn a second thread in which at least a portion of

the same program also executes, said second thread runs concurrently with the first thread, but ahead of the first thread in program order.

11. The processor of claim 10 wherein said instructions that cause a second thread to be spawned include a start instruction which causes the second thread to start and a stop instruction which causes the second thread to stop.

12. The processor of claim 11 wherein said start instruction includes a value designating the location in the program where the second thread is to start running.

13. The processor of claim 10 wherein the second thread encounters a cache miss condition for a memory reference but the first thread does not encounter a cache miss condition when that same memory reference is processed by the first thread.

14. The processor of claim 10 wherein said processor determines whether sufficient hardware resources are available before spawning said second thread.

15. The processor of claim 10 wherein said processor ignores exception conditions generated during the second thread.

16. The processor of claim 10 wherein said processor does not permit a store instruction in the second thread to modify data cache contents.

17. The processor of claim 10 wherein said processor does not permit any store instruction in the second thread to modify data cache contents.

18. The processor of claim 10 further including a buffer into which pre-execution thread store data is written to make such store data available to pre-execution thread load instructions.

19. A method of running a program in a processor, comprising:

(a) inserting pre-execution thread instructions in the program;

(b) spawning a pre-execution thread when designated by the inserted instructions; and

(c) running said pre-execution thread concurrently with a main thread wherein both the pre-execution and the main threads include instructions from the same program, the pre-execution thread running ahead of the main thread.

20. The method of claim 19 further including stopping the pre-execution thread when designated by the inserted instructions in (a).

21. The method of claim 19 further including copying register contents associated with the main thread to registers used by the pre-execution thread.

22. The method of claim 19 further including determining whether sufficient hardware resources are available to spawn the pre-execution thread.

23. The method of claim 19 further including ignoring all exception conditions generated during the pre-execution thread.

24. The method of claim 19 further including not permitting a store instruction in the pre-execution thread to modify memory contents.

25. The method of claim 19 further including copying the contents of at least one register to memory to make such contents available to the pre-execution thread.

26. The method of claim 19 further including writing pre-execution store data into a buffer that can be accessed by a pre-execution load instruction.

27. The method of claim 19 further including not permitting any store instruction in the pre-execution thread to modify memory contents.

28. The method of claim 19 wherein (a) includes inserting a start instruction which causes the processor to start the pre-execution thread.

29. The method of claim 19 wherein the start instruction specifies a location in the program at which the pre-execution thread is to start running.

30. The method of claim 19 wherein (a) includes inserting a stop instruction which causes the processor stop the pre-execution thread.

31. A processor, comprising:

a fetch unit capable of fetching instructions from a plurality of threads;

a program counter coupled to said fetch unit;

an instruction cache coupled to said fetch unit;

a data cache coupled to said instruction cache;

wherein said processor pre-executes instructions from a main thread.

32. The processor of claim 31 wherein a pre-execution thread is caused to be spawned to pre-execute said instructions by an instruction in the main thread.

33. The processor of claim 31 wherein a pre-execution thread spins on a variable that is set to a predetermined value by the main thread when there are instructions to pre-execute.

34. The processor of claim 31 wherein the processor ceases pre-executing instructions when a program counter is encountered that exceeds a range.

35. The processor of claim 31 wherein the processor ceases pre-executing instructions when the main thread catches up to the pre-executing instructions.

36. The processor of claim 31 wherein the processor ceases pre-executing instructions when the number of pre-executing instructions exceeds a limit.